IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the Application:

LISTING OF CLAIMS:

1. (Currently Amended) In a computerized device, a method for controlling speculative execution of instructions, the method comprising the steps of:

detecting a multiaccess memory condition based on a reference to a memory location common to a plurality of page table entries, the page table entries each corresponding to at least a first processor and a second processor;

setting a value of a speculation indicator based on the multiaccess memory condition to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location;

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allowing speculative execution of instructions in a processor in the computerized device; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allowing speculative execution of instructions in the processor in the computerized device.

2. (Currently Amended) The method of claim 1 wherein the step of detecting a multiaccess memory condition comprises the steps of:

identifying a potential of thea first processor to access thea memory location;

identifying a potential of thea second processor to concurrently access the memory location; and

wherein in response to the steps of identifying, the step of setting a value of a speculation indicator comprises the step of setting the value of the

speculation indicator to indicate that speculative execution of instructions by at least one of the first and second processors is not allowed in the computerized device for instructions that reference the memory location.

3. (Currently Amended) The method of claim 2 wherein the step of identifying a potential of a first processor to access a memory location comprises the step of:

detecting an access, by the first processor, to thea page table entry of a page table associated with the first processor, the page table entry containing an association to the memory location; and

retrieving the access to the page table entry; and

wherein the step of identifying a potential of a second processor to access the memory location comprises the steps of:

comparing the content of the access to the page table entry of the first processor to a set of page table entries associated with the second processor to identify thea page table entry associated with the second processor that references the memory location associated with the access to the page table entry by the first processor.

4. (Original) The method of claim 3 wherein the step of comparing the content of the access to the page table entry of the first processor to a set of page table entries associated with the second processor comprises the step of:

detecting that a page table entry referenced by the access to the page table entry of the first processor matches a page table entry contained in a translation lookaside buffer associated with the second processor.

5. (Original) The method of claim 2 wherein the step of identifying a potential of a first processor to access a memory location comprises the step of:

retrieving an access to a page table entry by a first processor;

wherein the step of identifying a potential of a second processor to access the memory location comprises the step of:

detecting that the page table entry accessed by the first processor matches a page table entry referenced by a memory management unit of the second processor; and

wherein the speculation indicator is associated with the matching page table entry referenced by a memory management unit of the second processor; and

in response to the steps of retrieving and detecting, the step of setting a value of a speculation indicator comprises the step of:

setting a speculation indicator associated with the page table entry referenced by a memory management unit of the second processor to indicate that speculative execution of instructions is not allowed for instructions executed by the second processor that reference memory referenced by the page table entry.

6. (Original) The method of claim 1 wherein the step of detecting a multiaccess memory condition comprises the step of:

detecting when at least two processors in the computerized device have a potential to execute instructions that reference locations within a shared page of memory.

7. (Original) The method of claim 6 wherein the step of detecting when at least two processors in the computerized device have a potential to execute instructions that reference locations within a common page of memory comprises the steps of:

monitoring a first processor translation lookaside buffer reference to a page table associated with a first processor;

comparing the first processor translation lookaside buffer reference to a set of translation lookaside buffer references associated with a second processor; and

setting a value of the multiaccess memory condition to indicate that speculative execution of instructions is not allowed by at least the second processor if the first processor translation lookaside buffer reference is associated with memory reference by at least one translation lookaside buffer reference associated with the second processor.

8. (Original) The method of claim 1 wherein the step of detecting a multiaccess memory condition comprises the step of:

identifying when a translation lookaside buffer span associated with a first processor overlaps a translation lookaside buffer span associated with at least one second processor; and

in response to the step of identifying, the step of setting a value of a speculation indicator based on the multiaccess memory condition comprises the step of:

setting the value of the speculation indicator to indicate that speculative execution of instructions is not allowed for portions of the translation lookaside buffer that overlap with one another.

9. (Original) The method of claim 8 wherein:

the speculation indicator is associated with a page table entry containing a reference to memory referenced by at least one instruction operating on the processor in the computerized device;

the step of setting the value of the speculation indicator sets the value of the speculation indicator to indicate that speculative execution of instructions is not allowed in the computerized device for pages of memory referenced by translation lookaside buffer entries in at least two processor in the computerized device;

and wherein the step of not allowing speculative execution of instructions in the computerized device comprises the steps of:

disallowing speculative execution of instructions by a processor in the computerized device if a speculation indicator associated with any page table entries that contain references to memory referenced by instructions to be executed in that processor indicate that speculative execution of instructions is not allowed in the computerized device.

10. (Currently Amended) In a computerized device, a method for controlling speculative execution of instructions, the method comprising the steps of:

detecting a multiaccess memory condition, detecting a multiaccess memory condition further comprises:

identifying when a translation lookaside buffer span associated with a first processor overlaps a translation lookaside buffer span associated with at least one second processor; and

setting a value of a speculation indicator based on the multiaccess memory condition;

in response to the step of identifying, the step of setting a value of the speculation indicator based on the multiaccess memory condition comprises the step of:

setting the value of the speculation indicator to indicate that speculative execution of instructions is not allowed for portions of the translation lookaside buffer that overlap with one another;

allowing, if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, speculative execution of instructions in a processor in the computerized device; and

disallowing, if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, speculative execution of instructions in the processor in the computerized device;

the speculation indicator being associated with a page table entry containing a reference to memory referenced by at least one instruction operating on the processor in the computerized device;

the step of setting the value of the speculation indicator includes setting the value of the speculation indicator to indicate that speculative execution of instructions is not allowed in the computerized device for pages of memory referenced by translation lookaside buffer entries in at least two processor in the computerized device;

the step of not allowing speculative execution of instructions in the computerized device further comprising:

disallowing speculative execution of instructions by a processor in the computerized device if a speculation indicator associated with any page table entries that contain references to memory referenced by instructions to be executed in that processor indicate that speculative execution of instructions is not allowed in the computerized device; and

~~The method of claim 9 wherein the step of not allowing speculative execution of instructions in the computerized device comprises the steps of~~ deactivating at least one speculative execution correction mechanism in the computerized device.

11. (Original) The method of claim 1 wherein the step of detecting a multiaccess memory condition comprises the step of:

determining when at least two processors in the computerized device do not have a potential to execute instructions that reference locations within a shared page of memory; and

in response to the step of determining, the step of setting a value of a speculation indicator comprises the step of setting the value of the speculation indicator to indicate that speculative execution of instructions is allowed in the computerized device.

12. (Original) The method of claim 1 wherein the step of setting a value of a speculation indicator based on the multiaccess memory condition comprises the steps of:

detecting a change in the value of the speculation indicator from a value indicating speculative execution of instructions is allowed in a processor in the computerized device to a value that indicates that speculative execution of instructions is not allowed in that processor in the computerized device; and

in response to the step of detecting a change in the value of the speculation indicator, performing a speculative execution recover operation for any instructions that have been speculatively executed and which are adversely affected by the change in the value of the speculation indicator.

13. (Original) The method of claim 1 wherein the step of detecting a multiaccess memory condition comprises the step of:

operating a multiprocessor cache coherency protocol to detect when a processor in the computerized device accesses a page table entry.

14. (Original) The method of claim 1 further comprising the step of executing instructions in the processor in the computerized device.

15. (Currently Amended) A processor configured to control speculative execution of instructions in a computerized device, the processor comprising:

an instruction orderer configured to receive and order a set of instructions for execution based on a speculation indicator;

an instruction executer coupled to the instruction orderer, the instruction executer configured to execute instructions in the set of instructions according to an order indicated by the instruction orderer;

a speculation indicator configured to receive and maintain a value that indicates if speculative execution of instructions is allowed in the processor; and

a speculative execution controller coupled to at least one of the instruction orderer and the instruction executer and coupled to the speculation indicator, the speculative execution controller configured to:

detect a multiaccess memory condition based on a reference to a memory location common to a plurality of page table entries, the page table entries each corresponding to at least a first processor and a second processor;

set a value of a speculation indicator based on the multiaccess memory condition to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location;

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allow speculative execution of instructions in the processor in a computerized device; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allow speculative execution of instructions in the processor in the computerized device.

16. (Currently Amended) The processor of claim 15 wherein when the speculative execution controller is configured to detect a multiaccess memory condition, the speculative execution controller is further configured to:

identify a potential of thea first processor in a computerized device to access a memory location;

identify a potential of the processor comprising the speculative execution controller to concurrently access the memory location; and

wherein when the speculative execution controller is configured to perform the operations of identifying, the speculative execution controller is configured to set the value of the speculation indicator to indicate that speculative execution of instructions by at least one of the first and second processors is not allowed in the computerized device for instructions that reference the memory location.

17. (Currently Amended) The processor of claim 16 wherein when the speculative execution controller is configured to identify a potential of thea first

processor to access a memory location, the speculative execution controller is configured to:

detect an access, by the first processor, to thea page table entry of a page table associated with the first processor, the page table entry containing an association to the memory location; and

retrieve the access to the page table entry; and

wherein when the speculative execution controller is configured to identify a potential of a second processor to access the memory location, the speculative execution controller is configured to:

compare the content of the access to the page table entry of the first processor to a set of page table entries associated with the second processor to identify a page table entry associated with the second processor that references the memory location associated with the access to the page table entry by the first processor.

18. (Original) The processor of claim 17 wherein when the speculative execution controller is configured to compare the content of the access to the page table entry of the first processor to a set of page table entries associated with the second processor, the speculative execution controller is configured to:

detect that a page table entry referenced by the access to the page table entry of the first processor matches a page table entry contained in a translation lookaside buffer associated with the second processor.

19. (Original) The processor of claim 16 wherein when the speculative execution controller is configured to identify a potential of a first processor to access a memory location, the speculative execution controller is configured to perform the operations of:

retrieving an access to a page table entry by a first processor;

wherein when the speculative execution controller is configured to identify a potential of a second processor to access the memory location, the speculative execution controller is configured to perform the operations of:

detecting that the page table entry accessed by the first processor matches a page table entry referenced by a memory management unit of the second processor; and

wherein the speculation indicator is associated with the matching page table entry referenced by a memory management unit of the second processor; and

in response to operations of retrieving and detecting, the operation of setting a value of a speculation indicator causes the speculative execution controller to be configured to perform the operation of:

setting a speculation indicator associated with the page table entry referenced by a memory management unit of the second processor to indicate that speculative execution of instructions is not allowed for instructions executed by the second processor that reference memory referenced by the page table entry.

20. (Original) The processor of claim 15 wherein when the speculative execution controller is configured to detect a multiaccess memory condition, the speculative execution controller is configured to:

detect when at least two processors in the computerized device have a potential to execute instructions that reference locations within a shared page of memory.

21. (Original) The processor of claim 20 wherein when the speculative execution controller is configured to detect when at least two processors in the computerized device have a potential to execute instructions that reference locations within a common page of memory, the speculative execution controller is configured to:

monitor a first processor translation lookaside buffer reference to a page table associated with a first processor;

compare the first processor translation lookaside buffer reference to a set of translation lookaside buffer references associated with a second processor; and

set a value of the multiaccess memory condition to indicate that speculative execution of instructions is not allowed by at least the second processor if the first processor translation lookaside buffer reference is associated with memory reference by at least one translation lookaside buffer reference associated with the second processor.

22. (Original) The processor of claim 15 wherein when the speculative execution controller is configured to detect a multiaccess memory condition, the speculative execution controller is configured to:

identify when a translation lookaside buffer span associated with a first processor overlaps a translation lookaside buffer span associated with at least one second processor; and

in response to such as identification, when the speculative execution controller is configured to set a value of a speculation indicator based on the multiaccess memory condition, the speculative execution controller is configured to:

set the value of the speculation indicator to indicate that speculative execution of instructions is not allowed for portions of the translation lookaside buffer that overlap with one another.

23. (Currently Amended) The processor of claim 2~~2~~3 wherein:

the speculation indicator is associated with a page table entry containing a reference to memory referenced by at least one instruction operating on the processor in the computerized device;

wherein when the speculative execution controller is configured to set the value of the speculation indicator, the speculative execution controller sets the value of the speculation indicator to indicate that speculative execution of instructions is not allowed in the computerized device for pages of memory referenced by translation lookaside buffer entries in at least two processor in the computerized device;

and wherein when the speculative execution controller is configured to not allow speculative execution of instructions in the computerized device, the speculative execution controller is configured to:

disallow speculative execution of instructions by a processor in the computerized device if a speculation indicator associated with any page table entries that contain references to memory referenced by instructions to be executed in that processor indicate that speculative execution of instructions is not allowed in the computerized device.

24. (Currently Amended) A processor configured to control speculative execution of instructions in a computerized device, the processor comprising:

an instruction orderer configured to receive and order a set of instructions for execution based on a speculation indicator;

an instruction executer coupled to the instruction orderer, the instruction executer configured to execute instructions in the set of instructions according to an order indicated by the instruction orderer;

a speculation indicator configured to receive and maintain a value that indicates if speculative execution of instructions is allowed in the processor; and

a speculative execution controller coupled to at least one of the instruction orderer and the instruction executer and coupled to the speculation indicator, the speculative execution controller configured to:

detect a multiaccess memory condition;

identify when a translation lookaside buffer span associated with a first processor overlaps a translation lookaside buffer span associated with at least one second processor; and

set a value of a speculation indicator based on the multiaccess memory condition;

in response to such as identification, when the speculative execution controller is configured to set a value of a speculation indicator based on the multiaccess memory condition, the speculative execution controller is configured to:

set the value of the speculation indicator to indicate that speculative execution of instructions is not allowed for portions of the translation lookaside buffer that overlap with one another; the speculative execution controller further configured to:

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allow speculative execution of instructions in the processor in a computerized device; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allow speculative execution of instructions in the processor in the computerized device, the speculation indicator being associated with a page table entry containing a reference to memory referenced by at least one instruction operating on the processor in the computerized device;

the speculative execution controller further configured to set the value of the speculation indicator, the speculative execution controller sets the value of the speculation indicator to indicate that speculative execution of instructions is not allowed in the computerized device for pages of memory referenced by translation lookaside buffer entries in at least two processor in the computerized device;

and wherein when the speculative execution controller is configured to not allow speculative execution of instructions in the computerized device, the speculative execution controller is further configured to:

disallow speculative execution of instructions by a processor in the computerized device if a speculation indicator associated with any page table entries that contain references to memory referenced by instructions to be executed in that processor indicate that speculative execution of instructions is not allowed in the computerized device; and

~~The processor of claim 23 wherein when the speculative execution controller is configured to not allow speculative execution of instructions in the computerized device comprises, the speculative execution controller~~ deactivates at least one speculative execution correction mechanism in the computerized device.

25. (Original) The processor of claim 15 wherein when the speculative execution controller is configured to detect a multiaccess memory condition by:

determining when at least two processors in the computerized device do not have a potential to execute instructions that reference locations within a shared page of memory; and

in response to determining, setting the value of the speculation indicator to indicate that speculative execution of instructions is allowed in the computerized device.

26. (Original) The processor of claim 15 wherein when the speculative execution controller is configured to set a value of a speculation indicator based on the multiaccess memory condition, the speculative execution controller is configured to:

detect a change in the value of the speculation indicator from a value indicating speculative execution of instructions is allowed in a processor in the

computerized device to a value that indicates that speculative execution of instructions is not allowed in that processor in the computerized device; and

in response to detecting a change in the value of the speculation indicator, performing a speculative execution recover operation for any instructions that have been speculatively executed and which are adversely affected by the change in the value of the speculation indicator.

27. (Original) The processor of claim 15 wherein the speculative execution controller is configured to detect a multiaccess memory condition by operating a multiprocessor cache coherency protocol to detect when a processor in the computerized device accesses a page table entry.

28. (Currently Amended) A speculative execution controller comprising:

an interface capable of coupling to an interconnection of a first processor, a second processor, and a memory system in a computerized device;

processing circuitry coupled to the interface configured to:

detect a multiaccess memory condition between the first and second processors via the first interface based on a reference to a memory location common to a plurality of page table entries, the page table entries each corresponding to at least a first processor and a second processor;

set a value of a speculation indicator in the memory system based on the multiaccess memory condition in the computerized device to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location;

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allow speculative execution of instructions in at least one of the first and second processors; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allow speculative execution of instructions in at least one of the first and second processors in the computerized device.

29. (Currently Amended) A computerized device comprising:

a memory system;

a first processor;

at least one second processor;

a speculative execution controller;

an interconnection mechanism coupling the first processor, the second processor, the memory system and the speculative execution controller;

wherein the speculative execution controller is configured to be capable of:

detecting a multiaccess memory condition between the first and second processors based on a reference to a memory location common to a plurality of page table entries, the page table entries each corresponding to at least a first processor and a second processor;

set a value of a speculation indicator in the memory system based on the multiaccess memory condition to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location;

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allow speculative execution of instructions in at least one of the first and second processors in the computerized device; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allow speculative execution of instructions in at least one of the first and second processors in the computerized device.

30. (Currently Amended) A computer program product having a computer-readable medium including computer program logic encoded thereon that, when performed in a computer device having a coupling of a memory system and at least two processors, programs a speculative execution controller to perform the operations of:

detecting a multiaccess memory condition between the first and second processors based on a reference to a memory location common to a plurality of page table entries, the page table entries each corresponding to at least a first processor and a second processor;

setting a value of a speculation indicator in the memory system based on the multiaccess memory condition to indicate that speculative execution of instructions by at least one of the first and the second processors is not allowed in the computerized device for instructions that reference the memory location;

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allow speculative execution of instructions in at least one of the first and second processors in the computerized device; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allow speculative execution of instructions in at least one of the first and second processors in the computerized device.

31. (New) The method of claim 9 wherein the step of not allowing speculative execution of instructions in the computerized device comprises the steps of deactivating at least one speculative execution correction mechanism in the computerized device.

32. (New) The processor of claim 23 wherein when the speculative execution controller is configured to not allow speculative execution of instructions in the computerized device comprises, the speculative execution controller deactivates at least one speculative execution correction mechanism in the computerized device.